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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,253	09/24/2003	Noriyuki Tanaka	24500-000007/US	4297

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HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195

EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 01/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,253	TANAKA ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/23/05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4 and 7-16* is/are rejected.

7)☒ Claim(s) *3,5 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-2, 4, 7-8, and 9-16 are rejected under 35 U.S.C. 102(a) as being anticipated by the admitted prior art.

Referring to claim 1: The prior art discloses a conversion between LSI and CPU (Specification, pages 3-4). The prior art discloses that the conversion interface between the LSI and CPU divides the wider bus width to accommodate the CPU's narrower bus width (Specification, page 3, lines 12-17). The prior art discloses dividing the LSI's bus width to accommodate the CPU's instruction (Specification, page 3, last paragraph); the prior art discloses dividing the 18-bit at least three times with various division patterns (Specification, page 3, 2nd paragraph, last 4 lines), which is the claimed setting section for setting the total number of transfer operations required for the first device to transfer the plurality of bit data groups and for setting a division pattern of the N-bit data for dividing the N-bit data into the plurality of bit data groups. The conversion interface's data receiving portion for receiving data from LSI is the claimed receiving section, and the conversion interface's data outputting portion for outputting data to CPU is the claimed output section. Hence, claim is anticipated by the admitted prior art.

Referring to claim 2: The prior art discloses dividing the 18-bit at least three times with various division patterns (Specification, page 3, 2nd paragraph, last 4 lines), and the prior art further discloses that CPU sets the division pattern (Specification, page 3, last paragraph), which are the claimed dividing the N-bit data into the plurality of bit data groups in accordance with the total number of transfer operations and the division pattern set by the setting section.

Referring to claim 4: The prior art discloses dividing the 18-bit at least three times with various division patterns (Specification, page 3, 2nd paragraph, last 4 lines), which is determining the total number of transfer operations and the division pattern in accordance with the size of the first bus width.

Referring to claim 7: The prior art discloses dividing the 18-bit at least three times with various division patterns (Specification, page 3, 2nd paragraph, last 4 lines); the prior art's means for selecting the division pattern is equivalent to the claimed second register. The prior art discloses the number of division may be more than three depending on CPU's logic (Specification, page 3, last paragraph); the prior art's means for selecting or setting the number of division is equivalent to the claimed first register for setting the total number of transfer operations.

Referring to claim 8: The admitted prior art discloses outputting to a monitor display, which is the claimed write access.

Referring to claim 9: The prior art discloses bi-directional communication between the CPU and LSI.

Referring to claim 10: The prior art discloses a conversion between LSI and CPU (Specification, pages 3-4). The prior art discloses that the conversion interface between the LSI

and CPU divides the wider bus width to accommodate the CPU's narrower bus width (Specification, page 3, lines 12-17). The prior art discloses dividing the LSI's bus width to accommodate the CPU's instruction (Specification, page 3, last paragraph); the prior art discloses dividing the 18-bit at least three times with various division patterns (Specification, page 3, 2nd paragraph, last 4 lines). The prior art's various division pattern is the claimed setting section for setting the total number of transfer operations required for the first device to transfer the plurality of bit data groups and for setting a division pattern of the N-bit data for dividing the N-bit data into the plurality of bit data groups. The prior art's means for dividing the LSI's bus width is the claimed dividing section for dividing the N-bit data into the plurality of bit data groups in accordance with the total number of transfer operations and the division pattern. Hence, claim is anticipated by the admitted prior art.

Referring to claim 11: The prior art discloses outputting the divided/converted data to the CPU, which is the claimed outputting the plurality of bit data groups to the first device in data read access from the second device to the first device.

Referring to claim 12: The prior art discloses bi-directional communication between the LSI and CPU.

Referring to claim 13: The prior art discloses a conversion between LSI and CPU (Specification, pages 3-4). The prior art discloses that the conversion interface between the LSI and CPU divides the wider bus width to accommodate the CPU's narrower bus width (Specification, page 3, lines 12-17). The prior art discloses dividing the LSI's bus width to accommodate the CPU's instruction (Specification, page 3, last paragraph); the prior art discloses dividing the 18-bit at least three times with various division patterns (Specification,

page 3, 2nd paragraph, last 4 lines), which is the claimed setting section for setting the total number of transfer operations required for the first device to transfer the plurality of bit data groups and for setting a division pattern of the N-bit data for dividing the N-bit data into the plurality of bit data groups. The conversion interface's data receiving portion for receiving data from LSI is the claimed receiving section, and the conversion interface's data outputting portion for outputting data to CPU is the claimed output section. Hence, claim is anticipated by the admitted prior art.

Referring to claim 14: The prior art discloses a display apparatus (Specification, page 2, last paragraph).

Referring to claim 15: The prior art discloses a conversion between LSI and CPU (Specification, pages 3-4). The prior art discloses that the conversion interface between the LSI and CPU divides the wider bus width to accommodate the CPU's narrower bus width (Specification, page 3, lines 12-17). The prior art discloses dividing the LSI's bus width to accommodate the CPU's instruction (Specification, page 3, last paragraph); the prior art discloses dividing the 18-bit at least three times with various division patterns (Specification, page 3, 2nd paragraph, last 4 lines), which is the claimed setting section for setting the total number of transfer operations required for the first device to transfer the plurality of bit data groups and for setting a division pattern of the N-bit data for dividing the N-bit data into the plurality of bit data groups. The conversion interface's data receiving portion for receiving data from LSI is the claimed receiving section, and the conversion interface's data outputting portion for outputting data to CPU is the claimed output section. Hence, claim is anticipated by the admitted prior art.

Referring to claim 16: The prior art discloses a display apparatus (Specification, page 2, last paragraph).

Allowable Subject Matter

3. Claims 3 and 5-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Referring to claim 3: The prior arts on record do not explicitly disclose or teach a setting section as claimed having the advantage that the number of divisions and the division pattern can be arbitrarily set.

Referring to claim 5: The prior arts on record do not explicitly disclose or teach the claimed structure for a bus-width converting apparatus or method between a CPU and a displaying device.

Referring to claim 6: Claim is allowable because it incorporates the claim 5's allowable subject matter.

Response to Arguments

4. In response to Applicant's argument that the admitted prior art does not disclose a setting section (Remark, page 11, 4th paragraph, page 13, 4th and 5th paragraphs, page 14, 1st paragraph): The prior art discloses that the conversion interface between the LSI and CPU divides the wider bus width to accommodate the CPU's narrower bus width (Specification, page 3, lines 12-17).

The prior art discloses dividing the LSI's bus width to accommodate the CPU's instruction (Specification, page 3, last paragraph); the prior art discloses dividing the 18-bit at least three times with various division patterns (Specification, page 3, 2nd paragraph, last 4 lines), which is the claimed setting section. Applicant argues that the setting section as disclosed in the independent claims has the advantage that the number of divisions and the division pattern can be arbitrarily set (Remark, page 12, 3rd paragraph). However, the language of the independent claims' limitation is broadly drafted; it does not preclude the division pattern from being a fixed pattern as disclosed in the admitted prior art. The dependent claim 3's limitations supports Applicant's argument regarding the arbitrarily division setting, and Examiner has considered Applicant's argument with claim 3 accordingly.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-3628. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676 or on the central telephone number, (571) 272-2100. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests

to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Justin King
January 6, 2006

RERANA PERVEEN
SUPERVISORY PATENT EXAMINER
1/9/2006